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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,097	02/13/2004	Jae-jun Moon	Q77183	4555

22373 7590 07/09/2009

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
07/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,097	MOON ET AL.	
	Examiner	Art Unit	
	Jeffrey S. Zweizig	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9 and 11-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5-9 and 11-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

In new claims 11-13, there is no antecedent basis for "the start up circuit means". Correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 7, 9 and 11-13 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Lee (6,356,139).

Applicant's Prior Art Fig. 1 shows an output terminal node N12, a common node N11, a power source voltage Vcc, a grounded power source Vss, a first PMOS transistor MP11, a second PMOS transistor MP12, a first NMOS transistor MN13, a second NMOS transistor MN14 and a resistor R11 all connected as recited in claim 1.

Applicant's Prior Art Fig. 1 does not show a start-up capacitor as recited in claim 1, however, Applicant's Background of the Invention notes that start-up circuits are typically required with bias circuits such as that shown in Fig. 1. Furthermore, the body of cited Prior Art supports the notion that such bias circuits typically require start-up circuits.

Wu et al. Fig. 1 shows a similar bias circuit wherein components M1, M2, M3 and M4 are analogous to components MP11, MP12, MN13 and MN14, respectively. Further shown is a star-up capacitor C1 as recited in claim 1. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect a capacitor as taught by Wu et al. between the output terminal node N12 and the common node N11 for the benefit of ensuring that the bias circuit properly starts. Moreover, all the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Applicant's Prior Art Fig. 1 does not specify a body connection as recited at the end of claim 1. Those of ordinary skill plainly understand that body connections are often schematically omitted for the sake of an uncluttered presentation. Where no body connection is shown, one conventionally assumes that the body is connected to the source because such a connection is the simplest, most straight forward way of terminating the body. Lee Fig. 1 shows a similar bias circuit wherein components P1, P2, N1, N2 and R1 are analogous to components MP11, MP12, MN13, MN14 and R11, respectively. Lee specifically shows that all the transistor bodies are connected to each of their respective sources. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect the bodies of the transistors to their respective sources for the benefit of terminating the bodies. Applicant's lack of a specific implementation invites the combination. This body connection scheme is further

supported by Fig. 8 as shown in Applicant's IDS reference 2002-237186. All the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 1 is obvious.

The output node outputs a constant bias voltage as recited in claim 5. Claim 5 is obvious.

Bias circuits exist for the very purpose of providing bias to another circuit outside the bias circuit. Claim 7 is obvious.

There is no difference seen between an "output terminal node" and an "output node". Claim 9 is otherwise identical to claim 1 and is obvious for the same reasons noted above.

Examiner's combination inherently possesses the properties recited in new claims 11-13.

Claims 3, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art Fig. 1 in view of Wu et al. (5,307,007) and Park et al. (5,880,625).

Applicant's Prior Art Fig. 1 shows an output terminal node N12, a second common node N11, a power source voltage Vcc, a grounded power source Vss, a third

PMOS transistor MP11, a fourth PMOS transistor MP12, a first NMOS transistor MN13, a second NMOS transistor MN14 and a resistor R11 all connected as recited in claim 3.

Applicant's Prior Art Fig. 1 does not show a second capacitor as recited in claim 3. Wu et al. Fig. 1 shows a second capacitor C1 as recited in claim 3. In would have been obvious to combine these elements as noted above.

Applicant's Prior Art Fig. 1 does not show the first and second PMOS transistors as recited in claim 3, however, such cascode circuit arrangements are well know as shown by the body of cited Prior Art. Park et al. Fig. 5 shows a specific example of a cascode bias circuit wherein components M56, M55, M52, M51 and R are analogous to components MP11, MP12, MN13, MN14 and R11, respectively. Park et al. shows additional cascode components in the form of a first PMOS transistor M54 and a second PMOS transistor M53. It would have been obvious to one of ordinary skill in the art at the time of the invention to augment Applicant's Prior Art Fig. 1 with cascode components M54 and M53 as taught by Park et al. for the benefit of, for example, reducing current fluctuations due to channel length modulation effects (col 4 ln 20). According to Examiner's combination, the junction of the gates of M54 and M53 form the claimed first common node. All the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

The Wu et al. reference also considers cascode circuit arrangements. Fig. 3, for example, shows common nodes and output nodes at the gate junctions of transistors

M3/M4, M5/M6 and M7/M8 with a capacitor connected between each pair of junctions. It would have been obvious to one of ordinary skill in the art at the time of the invention to connect a first capacitor as taught by Wu et al. between the first common node and the second common node and to connect a second capacitor as taught by Wu et al. between the second common node and the output node for the benefit of ensuring that the bias circuit properly starts. Moreover, all the claimed elements were known in the Prior Art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results to one of ordinary skill in the art at the time of the invention.

Claim 3 is obvious.

The output node outputs a constant bias voltage as recited in claim 6. Claim 6 is obvious.

Bias circuits exist for the very purpose of providing bias to another circuit outside the bias circuit. Claim 8 is obvious.

Response to Amendments and Arguments

In light of the amendments to the claims, the previous objections and 112 rejections are withdrawn.

The art rejections have been modified to reflect the cancellation of claim 4 and the addition of new claims 11-13.

In response to Applicant's arguments regarding claims 1, 3 and 9, Applicant's arguments are directed toward the Wu et al. reference by itself, not Examiner's combination. As pointed out above, Examiner's combination is seen to show all the limitations of claims 1, 3 and 9. Applicant does not appear to dispute the validity of Examiner's combination. Moreover, Applicant's arguments appear to have more to do with new claims 11-13 than claims 1, 3 and 9. Nevertheless, as pointed out above, Examiner's combination is seen to inherently possess the properties recited in new claims 11-13.

In response to Applicant's additional arguments regarding claim 3, Applicant points to Park et al Fig. 6, transistor M64. However, as can be seen above, Examiner's combination has nothing to do with Fig. 6 or M64. Nevertheless, none of Park et al. Figs. 1-7 show body connections as argued by applicant. As noted in column 5 lines 19-22, transistor M64 forms a current mirror with transistor M55, which indicates that transistor M64 is connected to the gate, not the body of transistor M55. Likewise, transistors M61, M62, M63 and M69 are all connected to the gates of M44, M46, M53 and M68, respectively.

Applicant's remaining argument is unclear. As best understood, applicant argues that both the Wu et al. and Park et al. references are directed toward stable (or reduced fluctuations of) current. It is not seen how this common attribute would cause the two references to be incompatible within the context of Examiner's combination. Moreover, both references show the same arrangement of stacked cascoded transistor pairs.

More Prior Art Notes

The attached PTO-892 shows yet another collection of references with commonly known arrangements of stacked transistor pairs and body connections.

Nicollini et al. (4,780,624) show that a bias output voltage may be extracted from any point within a bias circuit. This was a point of contention during the preceding Appeal attempt.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Wednesday 6:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeffrey S. Zweizig/
Primary Examiner, Art Unit 2816

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